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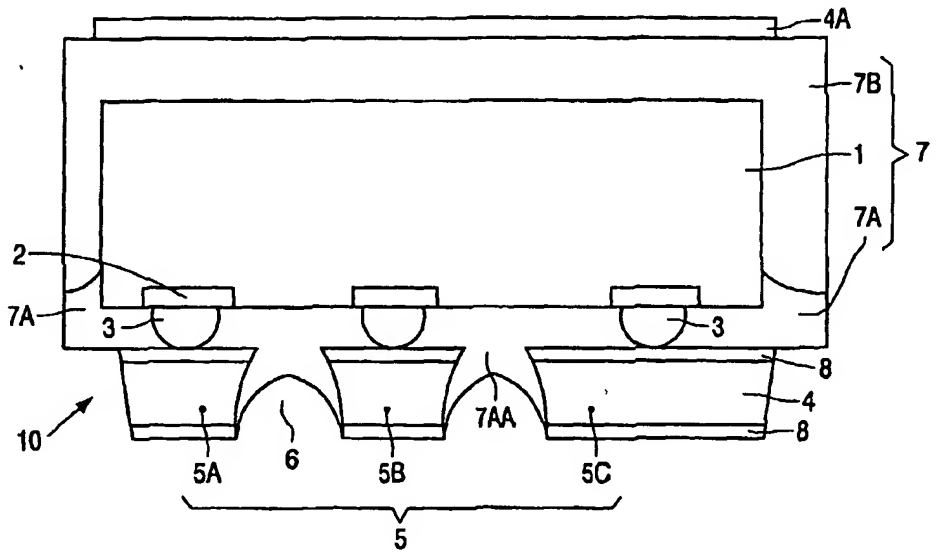

(57) Abstract: The method of manufacturing an electronic device (10) comprises the step of attaching an electric element (1) provided with connection regions (2) to a carrier (4) provided with a number of connection conductors (5A, 5B, 5C) by means of an electrically conducting connection (3) that is preferably of metal. Before the element (1) is attached to the carrier (4), a continuous electrically insulating layer (7A) is provided on the carrier (4), after which, during attachment of the element (1), the connection (3) is formed through the continuous insulating layer (7A). The thickness of the continuous insulating layer (7A) is preferably chosen to be such that during attachment of the element (1) onto the carrier (4), the space between the element (1) and the carrier (4) is filled completely. Subsequently, the remaining portion (7B) of the encapsulation (7) is provided.

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Method of manufacturing an electronic device

The invention relates to a method of manufacturing an electronic device comprising an electric element and a carrier, which electric element is provided, at a surface, with a number of connection regions, and which carrier is provided, at a surface, with a conductor pattern comprising a number of connection conductors, in which method the electric element is attached to the carrier in such a manner that the surfaces with the connection regions and the connection conductors face each other, and at least part of the connection regions and the connection conductors are electroconductively interconnected by electroconductive connections.

The invention also relates to a semiconductor device comprising a semiconductor element and a carrier, which semiconductor element is provided, at a surface, with connection regions and is substantially enveloped by an electrically insulating encapsulation, and which carrier is provided, at a surface, with a conductor pattern comprising connection conductors, at least part of said connection regions and connection conductors being mutually electroconductively connected by electroconductive connections, the surfaces of carrier and semiconductor element being held some distance apart while defining a cavity.

Such a method is known from the English-language abstract of Japanese patent specification JP-A-09027591, which was published on 28 January 1997. In said document a description is given of the way in which, in this case two, diodes are attached between two conductive plates, the anodes of the diodes being electroconductively connected to one carrier and the cathodes to the other carrier by means of soldering. After the diodes have been enveloped by an electrically insulating synthetic resin encapsulation provided between the plates, individual devices each comprising two diodes are obtained by means of sawing in two mutually perpendicular directions. The same technique is used to saw a groove in both plates between the (anodes and cathodes of the) diodes, which grooves extend just into the synthetic resin encapsulation. In this manner, a semiconductor device comprising, in

this case, a (semi)discrete semiconductor element is obtained in a very simple and inexpensive manner.

A drawback of the known method resides in that the reliability and service life of the devices obtained using said method are insufficient, which can be partly attributed to their compactness.

Therefore, a first object of the invention is to provide a method which (at least partly) obviates said drawback and which thus results in reliable devices which, in addition, are uncomplicated and inexpensive.

Said first object is achieved in that, prior to said attaching, a substantially uninterrupted electrically insulating layer is provided on a first one of the surfaces of the carrier and the electric element, after which attaching takes place by forming the electroconductive connections through the insulating layer, thereby causing the insulating layer to liquefy.

The invention is based on the surprising recognition that it is possible to form an electroconductive connection through an insulating layer if the insulating layer becomes liquid during the attaching operation. On account of the mass, the electric element or the carrier sinks through the insulating layer. As a result, it is possible to position the electric element on the carrier while at the same time the number of photolithographic steps remain limited. In addition, the combination of carrier and insulating layer provides for a good sturdiness. As a result of said sturdiness, the risk of cracks and mechanical stresses is reduced, resulting in an improved service life.

The electroconductive connection formed between the connection conductors and the connection regions provides for ohmic contact. The electroconductive connection is preferably formed by means of bumps, but alternatively electroconductive adhesive may be used for this purpose. Also, connection conductors and connection regions can be made in a thickness such that an adhesive layer on either one of them is sufficient to form the electroconductive connection.

It is an advantage of the invention that it can very suitably be used to carry out the attachment process on wafer-scale. In accordance with the state of the art, the encapsulation, which also envelops the electroconductive connection, is not provided until after a substrate has been separated into individual electric elements. Thus, if the attachment process is carried out on wafer-scale, the only mechanical support during the separation process is provided via the connections. As separating involves predominantly local mechanical stresses, there is a considerable risk of damage. In accordance with the invention,

the connections are enveloped already when the attachment process is carried out, so that improved mechanical stability is obtained.

In this connection, it is preferred that, prior to the attachment process, metal is provided on a second one of the surfaces, which metal forms the electroconductive connection when the attachment process is carried out at an increased temperature, and that the insulating layer contains a material that softens during said attachment process at said increased temperature. An example of a suitable material is an acrylate. Other thermoplastic synthetic resins are also suitable, as well as organic compounds having a suitable melting point. It is of course possible to add additives to the insulating layer, which are used, inter alia, to optimize the viscosity, the thermal coefficient of expansion, the capability of being softened and the thickness of the insulating layer. The metal is, for example, a solder or a bump of a metal such as gold, copper or silver.

It is an advantage of the invention that the insulating layer exerts an opposing force on the metal when the attachment process is carried out. Otherwise, the metal, which is slightly fluid when it is applied, may tend to sag out or spread over the carrier. Both effects are undesirable and lead to yield loss; the spread of metal may cause a short-circuit between neighboring connection conductors or connection regions. Sagging out of the metal may cause the conductive connection not to continue from connection regions to connection conductors. The device may also exhibit some degree of warpage since the connections are not all of the same length.

In a further modification, the connection conductors or connection regions are provided with an adhesive layer at the first one of the surfaces, which adhesive layer and the metal melt together when the attachment process is carried out. A favorable adhesive layer contains, for example, tin or platinum or gold or, possibly, lead.

In another embodiment, the insulating layer is applied in the liquid state, for example, by means of spin coating. In this case, the electric element must be attached to the carrier before the liquid has cured, or before the liquid reacts to form a more viscous or inelastic material, for example by polymerization. In this case, it is favorable if the liquid is viscous. Curing can take place, for example, by increasing the temperature for some time after the attachment process. This temperature step can also be used to improve the electroconductive connection between the connection conductors and the connection regions. Also in this case, the insulating layer may contain all sorts of additives.

In a favorable embodiment, the insulating layer is applied in a thickness such that, after the attachment process, said insulating layer substantially fills a cavity between the

surface of the electric element and the surface of the carrier. By means of this embodiment it is achieved that the reliability of the resultant electronic devices is improved since mechanical stresses and poor adhesion between the carrier and the element are precluded.

A suitable thickness of the insulating layer depends on the thickness of so-termed metal bumps or metal balls that may be present on the connection regions, and on the desired distance over which the side faces of the element must be covered, and on the quantity of the insulating layer that must be pressed into recesses that may be present in the carrier when the element is provided. Said quantity also depends on the dimensions of said recesses. Good results are obtained if the thickness of the uninterrupted insulating layer ranges between 15 and 60 μm.

In a further preferred embodiment, the insulating layer is provided at the surface of the carrier, and said carrier has recesses when the electric element is attached, and a part of the insulating layer is pressed into the recesses when the attachment process is carried out. It has been found that by forming recesses, the insulating layer is mechanically anchored in the carrier. As a result, the reliability is further increased.

The recesses in the carrier of this embodiment preferably extend as far as the opposite surface of the carrier. This has the advantage that the recesses can be formed in the carrier after the insulating layer has been applied. This is not necessary, however; the insulating layer may already penetrate the recesses when it is provided; furthermore, an insulating layer of a material that softens at a higher temperature can be applied as a foil. The synthetic resin foil then protects a surface of the carrier and, when the recesses are formed by means of etching, can be used as an etch-stop layer. If necessary, the shape of the recesses may be chosen to be such that still better anchoring of the insulating layer in the carrier is obtained when the element is provided, for example by providing the recesses with a conical shape such that the (truncated) tip of the cone is situated near the insulating layer. If necessary, the carrier may be provided with further recesses, for example in the form of round (conical) holes in the carrier, with a view to a good anchoring of the insulating layer. These holes can be formed concurrently with the recesses.

The carrier may be, inter alia, a metal foil, a stack of a number of metal layers, a multilayer substrate of a ceramic or polymer material with internal conductors, an electric component. For anchoring use can advantageously be made of a stack of at least two metal layers, which metal layers can be selectively etched. Below the metal layer at the surface, wherein the conductor pattern is defined, some degree of underetching may then occur. As a result, the conductor pattern is largely enveloped by the material of the liquefying insulating

layer, resulting in the conductor pattern being anchored. An additional advantage of a multilayer carrier is that it provides for good mechanical stability, in particular if pressure must be exerted during the attachment process.

In a further embodiment, a semiconductor element is chosen as the electric element, and part of the semiconductor element is removed from a surface of the semiconductor element situated opposite the surface provided with the connection regions. By virtue thereof, the compactness of the device obtained is further increased without the reliability being adversely affected. In connection with this, preferably, in a favorable modification of this embodiment, the semiconductor element chosen is a semiconductor element that comprises a further electrically insulating layer that separates the part of the semiconductor element from a further part that comprises the active part of the semiconductor element and that is provided with the connection regions. This insulating layer, which contains for example an oxide, can be used as an etch-stop layer when the part of the semiconductor element is removed. If the thickness of the uninterrupted insulating layer is suitably chosen, a method in accordance with the invention has the additional advantage that the side faces of the further (active) part of the semiconductor element are covered by a further part of the uninterrupted insulating layer after the semiconductor element has been attached. Preferably, also said part of the semiconductor element is removed then by chemical-mechanical polishing or etching, the last part of the removal process preferably being carried out by means of etching.

After attaching the electric element and the possible removal of a part thereof, it is favorable to provide an enveloping layer which, together with the insulating layer, substantially envelops the electric element. In this manner, the electric element is entirely enveloped, as is very customary for semiconductor elements. The enveloping layer comprises, for example, an epoxy material and may be provided by means of, for example, a suitable injection mold. In a favorable modification, after the semiconductor element has been attached to the carrier, a further carrier is provided above the semiconductor element, after which the enveloping layer is provided between the carrier and the further carrier preferably by means of injection molding. This embodiment provides for additional sturdiness and is particularly suitable for discrete semiconductor elements.

Favorable results are obtained if the thickness of the carrier and the thickness of the further carrier are chosen to range between 2 and 40 μm. Preferably, the thicknesses chosen for the carrier and the further carrier (4, 4A) are approximately the same. Preferably a copper foil is chosen for the carrier and the further carrier. This copper foil can be provided

with a tin layer on both surfaces, preferably, by means of a so-termed plating process. By virtue thereof, the metal connection can be established more readily and the device obtained is suitable for final assembly by means of a further metal connection.

It is also favorable if various electric elements are provided on the carrier, and, after providing the enveloping layer, the assembly is divided into individual electronic devices. In this case, the enveloping layer is provided at the level of the carrier, thereby reducing the amount of assembly work.

Alternatively, the semiconductor element to be provided may be part of a substrate with a plurality of semiconductor elements, and after attaching the substrate to the carrier, the assembly may be divided into individual electronic devices. This embodiment is particularly favorable if part of the substrate is removed from the semiconductor elements and, subsequently, an insulating carrier is provided. An example of such an insulating carrier is a glass carrier. After said separation, a stack comprised of the carrier, the insulating layer, the semiconductor element and the substrate is thus obtained. If the side faces of the semiconductor element are substantially composed of an electrically insulating material, a sufficiently enveloped semiconductor element is thus obtained without a synthetic resin encapsulation being present at the side faces. In this manner, a semiconductor element having a very small surface area is obtained. This embodiment can further be advantageously applied if the carrier comprises a plurality of electric elements, i.e. to manufacture chip-on-chip devices.

It is a second object of the invention to provide a semiconductor device of the type mentioned in the opening paragraph, which is reliable and can be embodied so as to have a very small thickness.

This second object is achieved in that the electrically insulating encapsulation comprises a first portion and a second portion, which first portion fills the cavity and encloses the electroconductive connections, and which second portion extends at the surface of the semiconductor element opposite the surface provided with connection regions.

The semiconductor element chosen can be a discrete or semi-discrete semiconductor element, but the invention can also very advantageously be applied for the manufacture of ICs (= Integrated Circuits), in particular the so-termed QFN (= Quad Flat No lead) type. The electric element is preferably provided with a synthetic resin encapsulation,

for example of an epoxy material. Alternatively use can be made of a ceramic encapsulation or a glass encapsulation or of a protective layer.

The carrier is, for example, a copper foil which is provided, at the surface with the connection conductors, with tin as the adhesive layer. Alternatively, the carrier may be composed of a stack of different layers, such as a layer of Al and a layer of Cu, a three-layer stack of Cu-Al-Cu, Cu-FeNi-Cu, FeNi-Cu-Ni, a multilayer laminate or a ceramic substrate. If a combination of copper and Al or FeNi is used, it is favorable if some degree of underetching occurs below the Cu at the surface with the connection conductors. This provides for further improved adhesion. As described in the non-prepublished application (PHNL020318) it is favorable to use a combination of Cu and Al, Al being etched away after the electric element has been enveloped. It is also possible that such a carrier includes an angle, in which case the carrier extends on two sides of the electric element.

The carrier may alternatively be or comprise an electric element. An example of a suitable electric element is a network of passive components. Such a network may be situated on a semiconductor substrate or a ceramic substrate. Another example is an integrated circuit for memory purposes, also referred to as memory chip. In this case, the result is a so-termed chip-on-chip connection.

Preferably, the surface area of the carrier is larger than that of the electric element. By virtue thereof, the carrier can be used as an interposer: part of the connection conductors is not connected to the connection regions of the electric element, but is used as a connection to, for example, a printed circuit board. Said larger surface area additionally enables various electric elements to be placed on the carrier so as to form a module, for example a multichip module or a power amplifier module. In this case, it may be favorable if the carrier is a multilayer substrate wherein passive components are defined. Said larger surface area further enables the encapsulation operation to be carried out at plate level before the carrier is separated into individual elements.

These and other aspects of the invention are apparent from and will be elucidated with reference to two embodiments described hereinafter.

In the drawings:

Fig. 1 is a diagrammatic cross-sectional view at right angles to the thickness direction of a semiconductor device manufactured by means of a first embodiment of a method in accordance with the invention,

Figs. 2 through 6 are diagrammatic cross-sectional views in the thickness direction of the device shown in Figure 1 in successive stages in the manufacturing process carried out by means of a first embodiment of a method in accordance with the invention,

Fig. 7 is a diagrammatic cross-sectional view at right angles to the thickness direction of a semiconductor device manufactured by means of a second embodiment of a method in accordance with the invention, and

Figs. 8 through 10 are diagrammatic cross-sectional views in the thickness direction of the device shown in Fig. 7 in successive stages of the manufacturing process carried out by means of a second embodiment of a method in accordance with the invention.

The Figures are not drawn to scale and some dimensions, such as the dimensions in the thickness direction, are exaggerated for clarity. Corresponding areas or parts are indicated by means of the same reference numerals whenever possible.

Fig. 1 is a diagrammatic cross-sectional view at right angles to the thickness direction of a semiconductor device manufactured by means of a first embodiment of a method in accordance with the invention. Figs. 2 through 6 diagrammatically show, in a corresponding cross-sectional view in the thickness direction, the device shown in Fig. 1 in successive stages of the manufacturing process carried out by means of a first embodiment of a method in accordance with the invention. A device 10 (see Fig. 1) comprises a semiconductor element 1 which is provided with a number of connection regions 2, three of which are shown in Fig. 1, which semiconductor element is situated, in this example, between a first and a second electroconductive carrier 4, 4A and is attached to the first carrier 4 by means of a metal connection 3 situated, in this case, directly above each connection region 2. In this case, both carriers 4, 4A are made of copper and have a thickness of 10 μm, the first carrier 4 being provided on both surfaces with an approximately 2 μm thick tin layer 8. In the first carrier 4 there is formed a conductor pattern 5 which comprises, in this case three, connection conductors 5A, 5B, 5C of the element 1. Between the carriers 4, 4A and around the semiconductor element 1 there is provided an electrically insulating encapsulation 7 that is comprised of two portions 7A,B. The first portion 7A contains, in this case, an acrylate and the second portion 7B contains an epoxy. The individual semiconductor device 10 comprising, in this example, a bipolar transistor 1 as the element 1, is formed by means of sawing in two mutually perpendicular directions, one of which extends parallel to the plane

of the drawing. The dimensions of the device 10 are, in this case, approximately 1 mm x 1 mm, and the height ranges between 0.3 and 0.5 mm.

The invention is manufactured as follows (see Figs. 2 through 6) by means of a first embodiment of a method in accordance with the invention. A carrier 4 of copper which is provided at both surfaces with a tin layer 8 is used as the starting element (see Fig. 2). At one surface there is subsequently provided an uninterrupted electrically insulating layer 7A, in this case a 25 μm thick layer of a synthetic resin 7A comprising, in this case, an acrylate foil 7A. The acrylate foil 7A is attached to the copper carrier 4 provided with tin layers 8 by exposing it to a small pressure and moderate heating. At the other surface of the carrier 4 a mask layer 20 is provided which comprises a photoresist layer 20 and which is patterned by means of photolithography so as to form the conductor pattern 5 which, in this case, comprises three connection conductors 5A, 5B, 5C for the semiconductor device 10 to be formed, which connection conductors are formed in this case by providing recesses 6, in this case two recesses 6, in the carrier 4. Said recesses are formed here by means of etching of, respectively, a tin layer 8, the copper carrier 4 and a further tin layer 8. It is noted that for clarity of the method as a whole, in Fig. 2 the carrier 4 is shown in inverted position with respect to the orientation used in this process step.

Subsequently, (see Fig. 3), a semiconductor element 1 is provided, in this case a bipolar transistor 1 with, in this case, three connection regions 2 on which metal balls 3 containing, in this case, gold are provided. The semiconductor element 1 is manufactured using customary semiconductor technology. In this process, the surface of the element 1 is provided with an insulating layer of silicon dioxide. The connection regions 2 are situated below apertures in the insulating layer and are provided with a metal layer onto which the metal balls 3 are attached. The element 1 is placed with its surface provided with metal balls 3 on the acrylate foil 7A, the device 10 to be formed being heated to 100 °C. In this process, the acrylate film 7A softens and the metal balls 3 sink to the surface of the carrier 4 where the metal connection 3 will be established. If necessary, use can be made of pressure means, not shown in the drawing, for example at the rear surface of the element 1. Also the heating means, which are positioned at the lower surface of the carrier 4, are not shown in the drawing.

Subsequently, (see Fig. 4), the device 10 to be formed is heated to 400 °C for a short period of time, in which process a metal connection 3 is formed, through the acrylate film 7A, between the element 1 and the tin-plated carrier 4. As, in this process, the height of the metal balls 3 decreases to 20 μm and the acrylate film 7A has a thickness of 25 μm, a part

7AA of the acrylate film 7A is pressed into the recesses 6 in the carrier 4. As a result, the film 7A is anchored in the carrier 4. In this case, an especially firm anchoring is obtained because the cross-section of the recesses 6 near the acrylate film 7A is smaller than the cross-section at the surface of the carrier 4 where the mask layer 20 is situated. Thus, between the element 1 and the carrier 4, an acrylate film 7A is present which is fully contiguous with the element 1, the metal balls 3 and the carrier 4. This has a very favorable effect on the reliability of the device 10. Also the anchoring of the acrylate film 7A in the carrier 4 contributes to this reliability. The dimensions of element 1 in this example are slightly less than 1 mm x 1 mm, and the thickness ranges between 200 and 380 μm. This comparatively small thickness can be achieved partly by removing a part from the rear surface of the element 1, i.e. a part of a semiconductor substrate present at said surface, for example by means of CMP (= Chemical Mechanical Polishing). The above-mentioned thickness of the device 10 can consequently vary as indicated hereinabove, but is comparatively small in any case.

Subsequently, (see Fig. 5), a further copper carrier 4A which, excepting the tin layers 8, is substantially identical to the carrier 4 is provided above the device 10 to be formed. The dimensions of the carriers 4, 4A are approximately 100 mm x 100 mm, so that a large number of devices 10, in this case approximately ten thousand, can be simultaneously manufactured. Next, a passivating synthetic resin is provided by means of an injection molding or filling technique between the carriers 4, 4A (akkoord ? zie Ned. tekst) and around the element 1 and the body 7. This synthetic resin comprises, in this case, an epoxy material and constitutes the enveloping layer 7B of the electrically insulating encapsulation 7 of the element 1. A very good adhesion between the two portions 7A, 7B of the encapsulation 7 is thus obtained.

Subsequently, see Fig. 6, a solid photoresist layer 60 is applied, in this case in a thickness of 5 microns, to the second carrier 4A. Using a suitable mask, this carrier is subsequently exposed so as to form apertures at the location of a saw cut to be formed for separating the devices 10 into individual devices. Subsequently, at the same locations parts of the first carrier 4 are removed in a manner similar to that indicated above. In this process, the portion 7B and the portion 7A of the encapsulation 7 are used as etch-stop layers. Subsequently, individual devices 10, as indicated in Fig. 1, are obtained which are suitable for surface mounting by sawing in two mutually perpendicular directions.

Fig. 7 is a diagrammatic cross-sectional view at right angles to the thickness direction of a semiconductor device manufactured by means of a second embodiment of a method in accordance with the invention. Figs. 8 through 10 diagrammatically show, in a

corresponding cross-section in the thickness direction, the device of Fig. 7 in successive stages of the manufacturing process carried out by means of a second embodiment of a method in accordance with the invention. The most important difference between the device 10 of Fig. 7 and the device 10 of Fig. 1 resides in that the former has a much smaller thickness. The thickness of the device shown in Fig. 7 is approximately 0.1 mm. This can be mainly attributed to a corresponding smaller thickness of the semiconductor element 1, which in this case is only approximately 10 μm.

The invention is manufactured as follows (see Figs. 8 through 10) by means of a second embodiment of a method in accordance with the invention. A carrier 4 (see Fig. 8) which, in this example, has the same configuration as in the first example is used as the starting element. Consequently, for the manufacture of the carrier 4 reference is made to the first example. The semiconductor element 1 having metal balls 3 is provided thereon. In this case, the semiconductor element is composed of two parts: a part 1A comprising, in this case, a monocrystalline silicon crystal 1A, and a part 1B comprising, in this case, a monocrystalline silicon layer 1B wherein the active part 1B including, in this case, the base, the emitter and the collector of a bipolar transistor is comprised, which active part has three connection regions 2 for the transistor. In this case, parts 1A, 1B are separated from each other by means of an electrically insulating layer 70 of silicon dioxide. This layer is formed, in this case, by shooting oxygen ions into a monocrystalline silicon crystal 1 by means of high energy ion implantation. The element 1 is attached to the carrier 4 by means of a metal connection 3 in a manner similar to that used in the previous example.

Subsequently, (see Fig. 9), the part 1A of the element 1 is removed by etching. As is shown in the Figure, in this process the side faces of the part 1B of the element 1 are protected against attack by the etchant, in this case an aqueous solution of potassium hydroxide, said protection being obtained by pressing a portion 7A,B of the acrylate film 7A against the side faces of the element to beyond the insulating layer 70 when the element 1 is being attached.

Subsequently, (see Fig. 10), the manufacturing process is continued as discussed with respect to the previous example, after which the device 10 of Fig. 7 is obtained, which is very compact and ready for mounting.

The invention is not limited to a method as described in the example, and within the scope of the invention many variations and modifications are possible to those skilled in the art. For example, devices having a different geometry and/or other dimensions

can be manufactured. It is also possible to use different materials for, in particular, the carriers. It is further noted that small adaptations enable also heat dissipation to be improved.

It is expressly noted that the mechanical separation technique that can be used to shape the individual semiconductor devices includes, in addition to sawing, also cutting or breaking. In the latter two techniques, in principle, substantially no loss of material occurs, whereas sawing leads to a loss of material equal to the width of a sawing cut. The present invention will be used, inter alia, to manufacture very small devices, in which case sawing leads to a comparatively substantial loss of material.

It is further noted that also on one of the carriers, for example the first carrier, additional elements or components can be provided for example by means of soldering, in which case the carrier is provided with a suitable conductor pattern.

Finally, it is noted that although the above examples only relate to a discrete semiconductor element, the invention can also be used for, in particular, the manufacture of integrated semiconductor products. Particularly in the lateral directions, these semiconductor products may, and will, of course have larger dimensions than the semiconductor elements in the above-discussed examples.

CLAIMS:

1. A method of manufacturing an electronic device comprising an electric element and a carrier, which electric element is provided, at a surface, with a number of connection regions, and which carrier is provided, at a surface, with a conductor pattern comprising a number of connection conductors, in which method the electric element is attached to the carrier in such a manner that the surfaces with the connection regions and the connection conductors face each other, and at least part of the connection regions and the connection conductors are electroconductively interconnected by electroconductive connections, characterized in that, prior to said attaching, a substantially uninterrupted electrically insulating layer is provided on a first one of the surfaces of the carrier and the electric element, after which attaching takes place by forming the electroconductive connections through the insulating layer, thereby causing the insulating layer to liquefy.

2. A method as claimed in claim 1, characterized in that, prior to the attachment process, metal is provided on a second one of the surfaces, which metal forms the electroconductive connection when the attachment process is carried out at an increased temperature, and the insulating layer contains a material which softens at said increased temperature during said attachment process.

3. A method as claimed in claim 2, characterized in that the connection conductors or connection regions are provided with an adhesive layer at the first one of the surfaces, which adhesive layer and the metal melt together when the attachment process is carried out.

4. A method as claimed in claim 1, characterized in that the insulating layer is applied in a thickness such that, after the attachment process, said insulating layer fills a cavity between the surface of the electric element and the surface of the carrier.

5. A method as claimed in claim 1, characterized in that the insulating layer is provided at the surface of the carrier, and said carrier has recesses when the electric element

is attached, and a part of the insulating layer is pressed into the recesses when the attachment process is carried out.

6. A method as claimed in claim 1, characterized in that a semiconductor element is chosen as the electric element, and part of the semiconductor element is removed from a surface of the semiconductor element situated opposite the surface provided with the connection regions.

7. A method as claimed in claim 6, characterized in that a semiconductor element is chosen that comprises a further electrically insulating layer that separates the part of the semiconductor element from a further part that comprises the active part of the semiconductor element and that is or will be provided with the connection regions.

8. A method as claimed in claim 1 or 6, characterized in that after attaching the electric element and the possible removal of a part thereof, an enveloping layer is provided which, together with the insulating layer, substantially envelopes the electric element.

9. A method as claimed in claim 8, characterized in that various electric elements are provided on the carrier, and, after providing the enveloping layer, the assembly is divided into individual electronic devices.

10. A method as claimed in claim 6, characterized in that the semiconductor element to be provided forms part of a substrate with a plurality of semiconductor elements, and after the substrate has been attached to the carrier, the assembly is divided into individual electronic devices.

11. A method as claimed in claim 1 or 10, characterized in that the carrier comprises at least one electric element.

12. A semiconductor device comprising a semiconductor element and a carrier, which semiconductor element is provided, at a surface, with connection regions and is substantially enveloped by an electrically insulating encapsulation, and which carrier is provided, at a surface, with a conductor pattern comprising connection conductors, at least part of said connection regions and connection conductors being mutually

electroconductively connected by electroconductive connections, the surfaces of carrier and semiconductor element being held some distance apart while defining a cavity, characterized in that the electrically insulating encapsulation comprises a first portion and a second portion, which first portion fills the cavity and encloses the electroconductive connections, and which second portion extends at the surface of the semiconductor element that is opposite to the surface provided with connection regions.

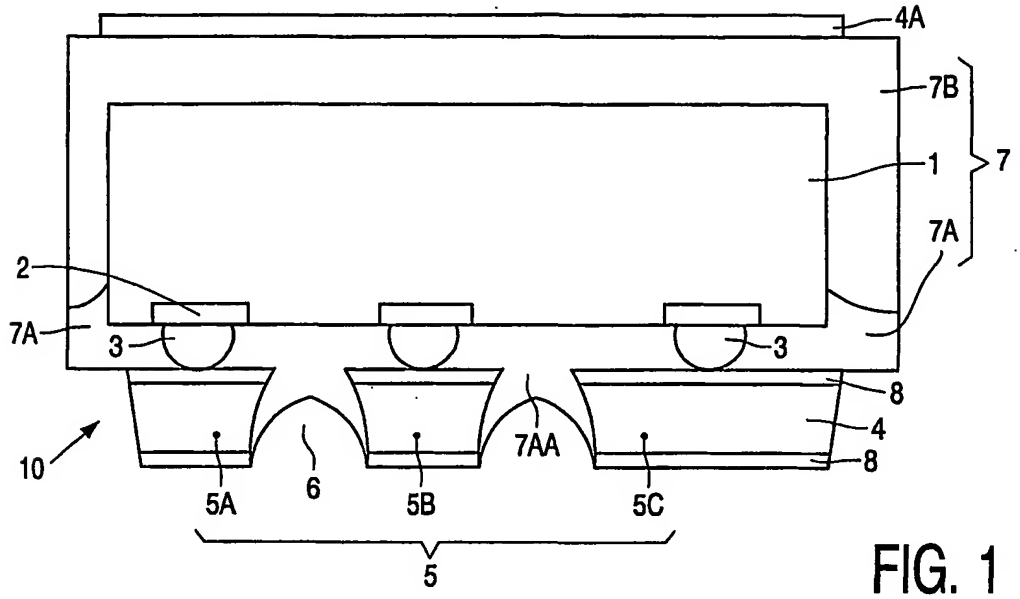

FIG. 1

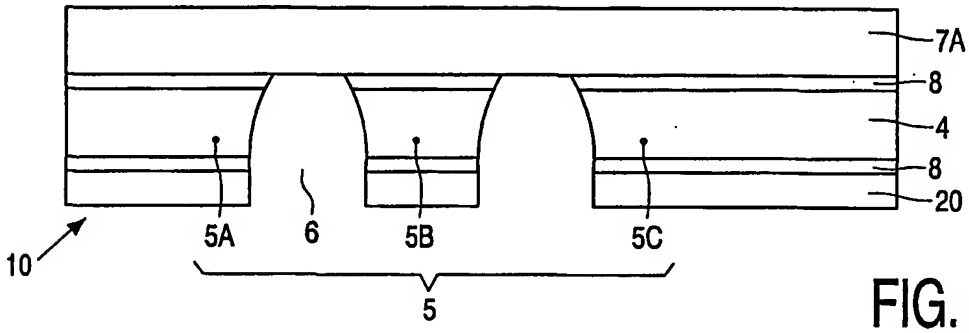

FIG. 2

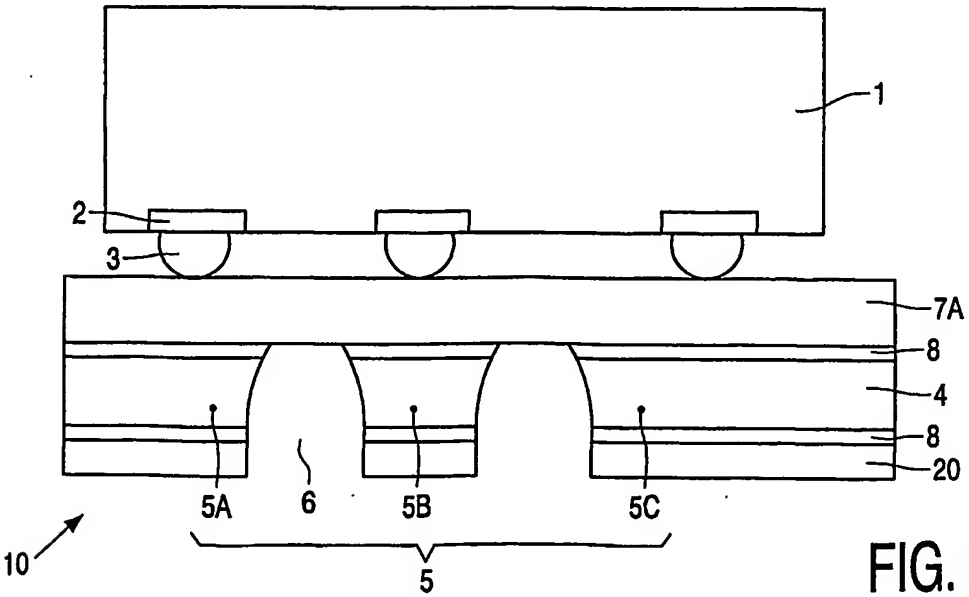

FIG. 3

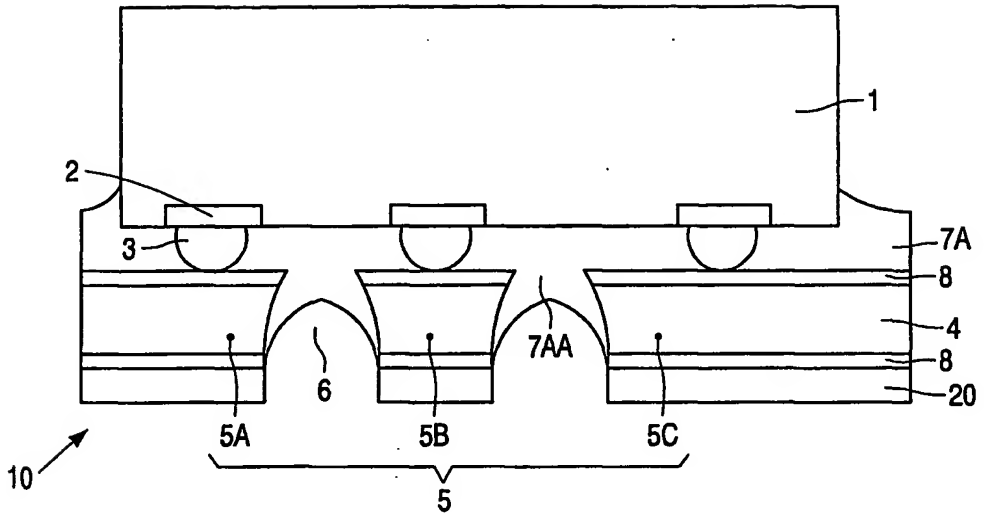
1
2
3
7A
8
4
7AA
8
6
20
5A
5B
5C
10
5

FIG. 4

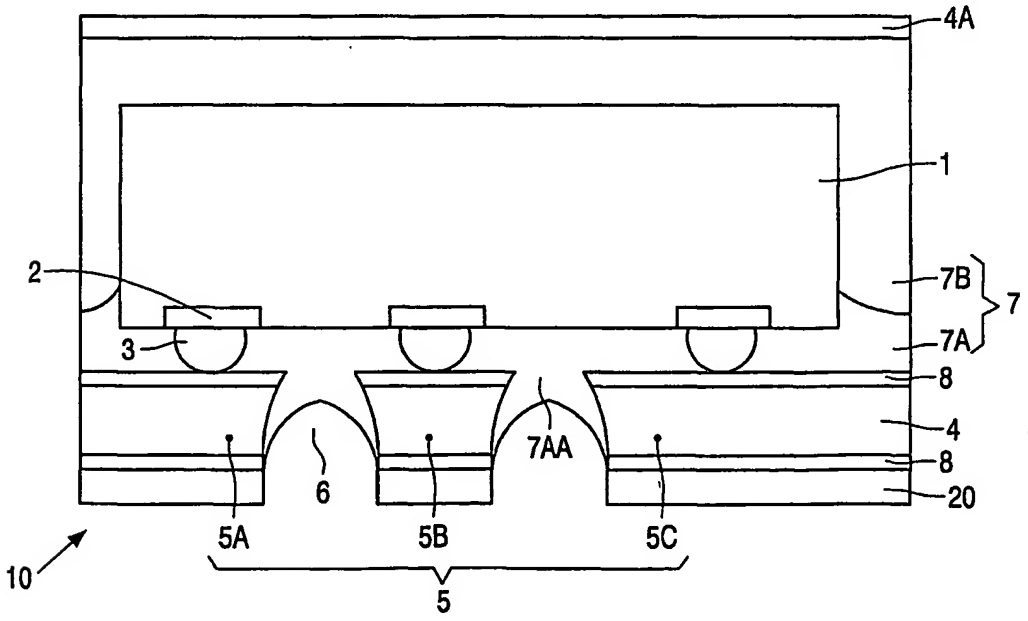
4A
1
2
7B
7
3
7A
8
4
7AA
8
6
20
5A
5B
5C
10
5

FIG. 5

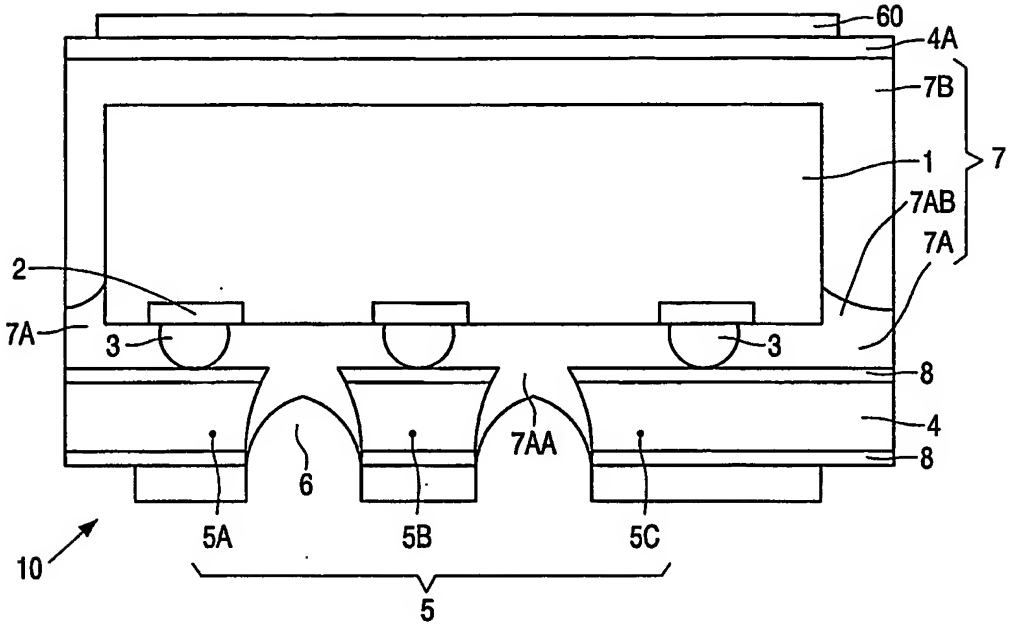
60
4A
7B
1
7
7AB
7A
2
7A
3
3
8
4
7AA
8
6
5A
5B
5C
10
5

FIG. 6

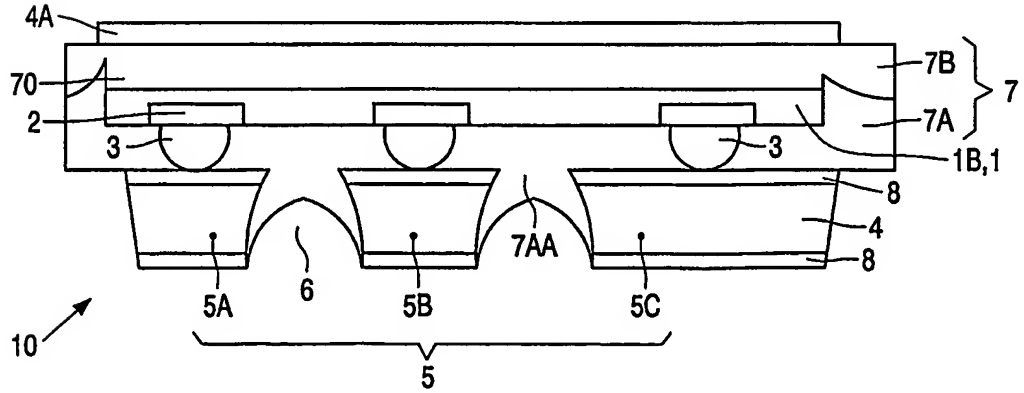
4A
7B
7
70
2
7A
3
3
1B,1
8
4
7AA
8
6
5A
5B
5C
10
5

FIG. 7

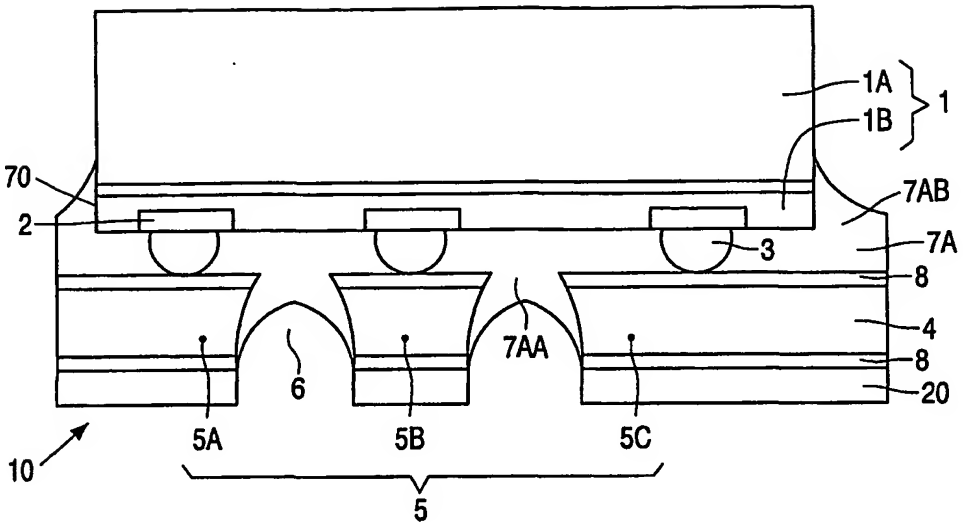

FIG. 8

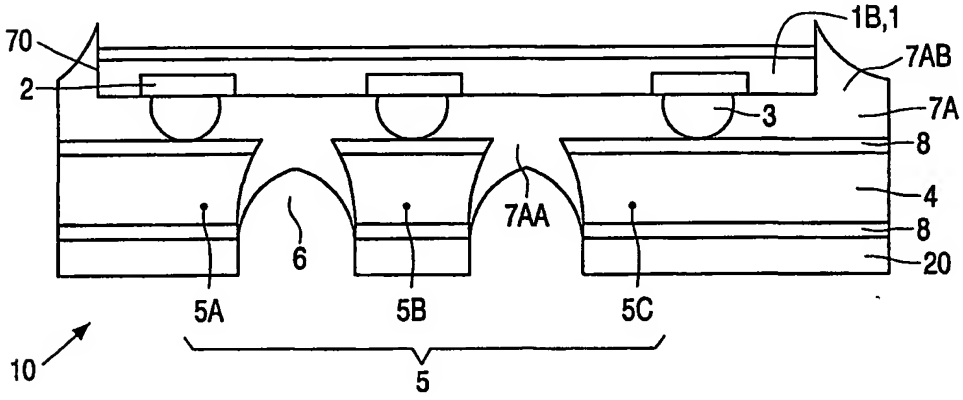

FIG. 9

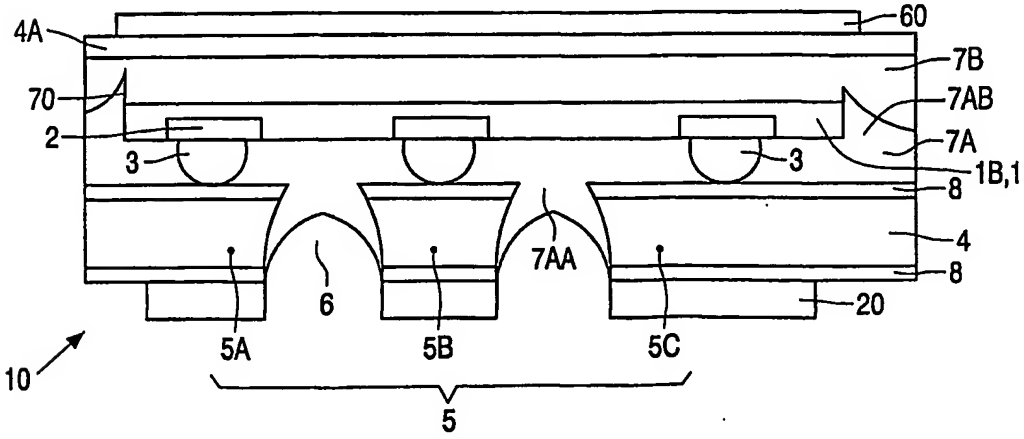

FIG. 10